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10/613,039	07/07/2003	Thomas Forest	0607 1455	5767
7590 02/06/2008 Dreiss, Fuhlendorf, Steimle & Becker			EXAMINER	
Postfach 10 37 62			BOLOURCHI, NADER	
Stuttgart, D-70032 GERMANY			ART UNIT	PAPER NUMBER
		·	2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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1		Application No.	Applicant(s)			
Office Action Summary		10/613,039	FOREST ET AL.			
		Examiner	Art Unit			
		Nader Bolourchi	2611			
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet with the c	orrespondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status			•			
1) 🏹	Responsive to communication(s) filed on 21 No	ovember 2007.				
		action is non-final.				
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
٠,٠	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
	·	reparte quayre, 1000 S.D. 11, 10				
Disposit	ion of Claims					
4)🖂	Claim(s) 1-6,9-15 and 17 is/are pending in the	application.	•			
•	4a) Of the above claim(s) is/are withdrawn from consideration.					
5)	Claim(s) is/are allowed.	•				
6)⊠	6)⊠ Claim(s) <u>1,2,4,5,9,10,12,13,15 and 17</u> is/are rejected.					
7)🖂	Claim(s) 3,6,11 and 14 is/are objected to.					
·	Claim(s) are subject to restriction and/or	election requirement.	•			
		·				
	on Papers					
9) ☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>07 July 2003</u> is/are: a) accepted or b)⊠ objected to by the Examiner.						
	Applicant may not request that any objection to the o	lrawing(s) be held in abeyance. See	e 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority ι	ınder 35 U.S.C. § 119	· ·				
	•	nriarity under 25 H.S.C. S. 440(a)	(4) ~~ (5)			
_	Acknowledgment is made of a claim for foreign	priority under 35 U.S.C. § 119(a)	-(a) or (i).			
a)	All b) Some * c) None of:		·			
	1. Certified copies of the priority documents					
	2. Certified copies of the priority documents have been received in Application No					
·	3. Copies of the certified copies of the priority documents have been received in this National Stage					
	application from the International Bureau (PCT Rule 17.2(a)).					
* See the attached detailed Office action for a list of the certified copies not received.						
		•				
	·		· · ·			
Attachmen	t(s)					
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date.						
_	, 🗀					
Pape	r No(s)/Mail Date	6)				

DETAILED ACTION

Remarks

- 1. Applicant's amendment to claims dated 11/21/2007 is entered.
- 2. Applicant canceling claims 7, 8, and 16 is acknowledged.
- 3. Specification objection is withdrawn.
- 4. Claim objections are withdrawn.
- 5. Claim Rejections under 35 USC § 112 is withdrawn.
- 6. Claims stand rejected under 35 USC § 102.
- 7. Claims stand rejected under 35 USC § 103.

Response to Arguments

- 8. Applicant's arguments filed 11/21/2007 have been fully considered but they are not persuasive.
- 9. In regards to claim 17, Applicant properly notes that (emphasis added):

"When functional descriptive material is recorded on some computer readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare in re Lowry, 32 F.3d 1579, 158384, 32 USPQ 2d 1031, 1035 (Fed Cir. 1994) (claim to data structure stored on a computer readable medium that increases computer efficiency held statutory").

However, Applicant fail to use the language, as underlined above, in the amended claim 17:

- 17. (currently amended) A data storage medium having machine encoded instructions stored thereon for executing the method of claim—1 which are executable by at least one of a computer and a microprocessor, the executable instructions comprising the steps of:
 - a) sampling a bit in a bit stream to generate at least two sample values of the bit;
 - b) defining a detecting window of sample values which are used to determine a value of the bit:
 - c) applying majority voting to the sample values within the detection window; and
 - d) generating a value of the sampled bit in dependence on results of step c).

However, a data storage does not necessary suggest that it is a "computer readable medium", as originally submitted in the Applicant's remarks. The above language does not even distinctively suggest that the storage is a part of computer, as Applicant argues. The preamble of the claim shown above, only suggests that the instructions are executable by a computer, i.e., "a computer program". Therefore claim 17 stand rejected under 35 USC § 101.

10. Regarding claims 1 and 9, Applicant provides the general overview of the reference in page 9: line 20 to page 10: line 21, to come to the conclusion that (emphasis added):

In contrast thereto, the instant invention as claimed is directely to a technique which is substantially simpler than that of Hedberg. Moreover, Hedberg presumably provides a different level of tolerance to errors than that of the instant invention.

In response to Applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., underlined above) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

11. Applicants further argues that (emphasis added):

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Hedberg transmits the data

words multiple times, decoding the bits of each of those copies, and then combing those decoded bits to make a higher level decision on the value of the bits in the original word, based on multiple compiled words. In contrast thereto, the method and associated device in accordance with the invention as claimed in claims 1, 9 and 17 inherently describes a process in which the data need only be transmitted once with a reception decision being made based on oversampling of that single data transmission. Seen in this manner, Hedberg is a higher level technique than that in accordance with the instant invention. The bit stream decoder in accordance with the instant invention is analogous to bit decision means of Hedberg for each bit of each of the redundant copies of the data.

Examiner respectfully disagrees with Applicant's observation, based on the following:

- In response to Applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **underlined above**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
- Examiner also notes that list of inventors and assignees include some of the Core Partners of FlexRay Consortium (see; http://www.flexray.com) (emphasis added):

Consortium continuation

The previous FlexRay Consortium agreements expired on December 31, 2005. To ensure seamless continuation of the FlexRay Consortium the seven Core Partners (BMW, Bosch, DaimlerChryster, Freescale, General Motors, NXP Semiconductors, Volkswagen) agreed on continuation agreements for the timeframe from January 1, 2006, until December 31, 2008.

However, for the purpose of clarification, the following example (See: http://en.wikipedia.org/wiki/Flexray) is used, which clearly indicates that FlexRay protocol used by Applicant does transmit the data multiple times, as extensively discussed by FlexRay Consortium members (emphasis added)

Clock [edit]

FlexRay system consists of a bus and processors (electronic control units, or ECUs). Each ECU has an independent clock. The clock drift must be no more than 0.15% from the reference clock, so the difference between the slowest and the fastest clock in the system is no greater than 0.3%.

This means that, if ECU-s is a sender and ECU-r is a receiver, then for every 300 cycles of the sender there will be between 299 and 301 cycles of the receiver. The clocks are resynchronized frequently enough to assure that this causes no problems.

Bits on the bus

Multiple transmission

[edit]

At each time, only one ECU writes to the bus. Each bit to be sent is held on the bus for 8 sample clock cycles. The receiver keeps a buffer of the last 5 samples, and uses the majority of the last 5 samples as the input signal.

Single-cycle transmission errors may affect results near the boundary of the bits, but will not affect cycles in the middle of the 8-cycle region.

Sampled bits

The value of the bit is sampled in the middle of the 8-bit region. The errors are moved to the extreme cycles, and the clock is synchronized frequently enough for the drift to be small. (Drift is smaller than 1 cycle per 300 cycles, and during transmission the clock is synchronized more than once every 300 cycles).

|000000|11111110000 |0000000|1111111|00

Correct averaging in case of no errors. The signal is merely delayed by 2 cycles.

|000000|111101110000 |00000000|1111111100

Errors near the middle of 8-cycle region are canceled.

00010|11111110000 0000001|111111100

Errors near the boundary of 8-cycle region may affect the boundary bit.

"bit cell"

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Here's an example of a particularly bad case - error during synchronization, a lost cycle due to clock drift and error in transmission.

Errors that happened in the example

- Because of a single-bit error during synchronization, the synchronization was delayed by 1 cycle
- Receiver clock was slower than sender clock, so receiver missed one cycle (marked X). This will not happen again before the next synchronization due
 to limits on maximum allowable clock drift.
- Because of a single-bit error during transmission, a bit was voted wrongly near the result.

Despite so many errors, the communication was received correctly.

The green cells are sampling points. All except the first are synchronized by the 1->0 edge in the transmission fragment shown.



- Examiner notes that Applicant in the specification in reference to FlexRay communication system, erroneously recites (emphasis added):

Typically, in a FlexRay communication system, <u>a bit comprises 8 or 10 samples, respectively,</u> a bit cell comprises 8 or 10 sample values.

- As discussed above, the phrase "a bit" should be replaced by the phrase a bit cell --, which is what Applicant referring to.

Applicant also argues (emphasis added):

Associated with this technical difference is the intrinsic property that the Hedberg patent relies on an underlying data rate of media which must be several times a resulting rate of usable decoded data. This is the case since the Hedberg technique relies on making individual low level bit decisions at the rate of bits on the link and the high level data is repeated multiple times to improve the probability of receiving a correct message in the presence of errors. For example, a word of 50 bits requires the Hedberg system to actually transmit 250 bits (five redundant copies of the same 50 bit word). Assuming, for example, this is conveyed in 5 µs, then the underlying data rate of the link must be 50 Mbit/s. This is necessary because each of the low level bits is independent and the link must therefore be capable of carrying data at the rate of the low level bits.

In contrast thereto, the technique in accordance with the invention is based on oversampling (sampling at a rate higher than the encoded rate on the link) with the intention of eliminating glitches that are shorter than a single bit. For the system in accordance with the invention, the same amount of data, i.e. 50 bits, conveyed in the same amount of time (5 µs) would require an underlying capability of only 10 Mbit/s, since the data is not repeated. In other words, in accordance with the method and device of the invention, although an oversampling is effected to make the bit decisions, the link itself must only carry data at the nominal bit rate.

In response to Applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., underlined above) are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

- 12. Furthermore, Applicant has amended claim 1, 9 and 17, by mainly adding the phrase; "sampling a bit in the received bit stream to generate, at least two sample values of said bit", in support of above remarks. As shown above, this is what Applicant discloses as "bit cell", which is result of multiple transition of the data, and is what Hedberg clearly discloses, as discussed above. Therefore claims 1, 9 and 17 stands rejected. It is recommended to replace the phrase " a bit" with the phrase - a bit cell -, in the aforementioned claims.
- 13. Examiner notes that Applicant is silent about the rejection of all dependent claims. Therefore, claims 1-6, 9-15, and 17 stand rejected.

Drawings

14. Figures 34 and 35 should be designated by a legend such as <u>--Prior Art--</u>because only that which is old is illustrated ,See MPEP § 608.02(g). ("Protocol Overview", FlexRay International Workshop, April 16, 2002, Munich, page 26; http://www.flexray.com/publications/intworkshop2002_04.pdf). Applicant is requested to check all the drawings against those disclosed in the presentations of FlexRay (located at http://www.flexray.com, under Publication section; such as one indicated above for Figs. 34-35) to properly designate all the old illustration as –prior art--. Corrected

drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

15. Claims 17 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Computer programs (as well as program in a computing unit and instruction stored in a data storage medium) claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer, which permit the computer program's functionality to be realized. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035. Since a computer program is merely a set of instructions capable of being executed by a computer, the

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computer program itself, without the computer-readable medium needed to realize the computer program's functionality, is not a process and claim for a computer program (as well as program in a computing unit and instruction stored in a data storage medium) is treated as nonstatutory functional descriptive material. Furthermore, as discussed above, a data storage does not necessary suggest that it is a "computer readable medium", as originally submitted in the Applicant's remarks. The above language does not even distinctively suggest that the storage is a part of computer, as Applicant argues. The preamble the claim 17 only suggests that the instructions are executable by a computer, i.e., "a computer program".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 16. Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Clark et al. (US 5,671,256).

Regarding claim 1. Clark discloses a method for bit stream decoding of a received bit stream (Fig. 4), the method comprising the steps of: a) sampling a bit in the received bit stream to generate, at least two sample values of said bit (Fig. 4: 41; Fig. 7; col. 3: lines

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23-32), (b) defining a detection window of sample values which are used to determine a value of said bit (Fig. 4: 42 and 43); c) applying a majority voting to said sample values within said detection window (Fig. 8; col. 4: lines 12-24; col. 6: line 66 – col. 7: line 14); d) generating a value of said sampled bit in dependence on the result of step C) (col. 4: lines 12-24), (e) decoding the bit stream using the bit values generated in step d) (Fig. 3; col. 3: lines 7-22; col. 4: lines 12-24).

Regarding claim 9, Hedberg discloses a device for decoding a received bit stream (Fig. 4), the device comprising: means for sampling a bit in the received bit stream to generate, at least two sample values of said bit (Fig. 4: 41; Fig. 7; col. 3: lines 23-32), means for defining a detection window of sample values which are used to determine a value of said bit(Fig. 4: 42 and 43); means for applying a majority voting to said sample values within said detection window (Fig. 8; col. 4: lines 12-24; col. 6: line 66 – col. 7: line 14); means for generating a value of said sampled bit in dependence on the result of said voting (col. 4: lines 12-24), (e) decoding the bit stream using the generated bit values (Fig. 3; col. 3: lines 7-22; col. 4: lines 12-24).

17. Claims 1, 4, 9, 12, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hedberg (US 5,995,559).

Regarding claim 1, Hedberg discloses a method for bit stream decoding of a received bit stream (Fig. 3), the method comprising the steps of: a) sampling a bit in the received

bit stream to generate, at least two sample values of said bit (col. 13: lines 13-23; Examiner notes that all signal processing operation in Fig. 3 is carried out by proper manipulation of digital samples of a received signal as recited in col. 14: lines 34-43), (b) defining a detection window of sample values which are used to determine a value of said bit(Fig. 8: 801, 802, 803, 804; col. 12: 23-29; Fig. 9; col. 12: lines 42-54, the detection windows is positioned by the data message detector Fig. 3: 7 as recited in col. 12: lines 31-33); c) applying a majority voting to said sample values within said detection window (col. 3: lines 48-62; Fig. 7A); d) generating a value of said sampled bit in dependence on the result of step C) (col. 13: lines 24-43), (e) decoding the bit stream using the bit values generated in step d) (col. 12: lines 14-22).

Regarding claim 4, Hedberg discloses as recited in rejection of claim 1 above. Hedberg also discloses said detection window is centered on an expected center of a bit cell of the bit stream to only overlap samples of said bit cell for detecting a bit value of said bit cell (Fig. 8: 801, 802, 803, 804; col. 12: 23-29; Fig. 9; col. 12: lines 42-54)

Regarding claim 9, Hedberg discloses a device for decoding a received bit stream (transceiver in Fig. 3), the device comprising: means for sampling a bit in the received bit stream to generate, at least two sample values of said bit (col. 13: lines 13-23; Examiner notes that all signal processing operation in Fig. 3 is carried out by proper manipulation of digital samples of a received signal as recited in col. 14: lines 34-43), means for defining a detection window of sample values which are used to determine a

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value of said bit(Fig. 8: 801, 802, 803, 804; Fig. 9; col. 12 lines 23-33; the detection windows is positioned by the data message detector Fig. 3: 7 as recited in col. 12: lines 31-33); means for applying a majority voting to said sample values within said detection window (col. 3: lines 48-62; Fig. 7A); means for generating a value of said sampled bit in dependence on the result of said voting (col. 13: lines 24-43), (e) decoding the bit stream using the generated bit values (col. 12: lines 14-22);

Regarding claim 12, Hedberg discloses as recited in rejection of claim 9 above. Hedberg also discloses said detection window is centered on an expected center of a bit cell of the bit stream to only overlap samples of said bit cell for detecting a bit value of said bit cell (Fig. 8: 801, 802, 803, 804; col. 12: 23-29; Fig. 9; col. 12: lines 42-54)

Regarding claim 15, Hedberg discloses as recited in rejection of claim 9 above.

Hedberg also discloses a node in a communication system, comprising the device of claim 9 (transceiver shown in Fig. 3)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- 18. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 19. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hedberg in view of Admitted Prior Art.

Regarding claim 2, Hedberg discloses as recited in rejection of claim 1 above. Hedberg is silent about number of sample being odd number.

Admitted Prior Art (Specification: page 3: line 2) discloses that the detection window can comprise any number of samples. Therefore, It would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teaching of Hedberg and admitted prior art for the purpose of having detection window with odd or even number of sample as suggested by Admitted Prior Art (Specification: page 3: line 2).

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Regarding claim 10, Hedberg discloses as recited in rejection of claim 9 above.

Hedberg is silent about number of sample being odd number.

Admitted Prior Art (Specification: page 3: line 2) discloses that the detection window can comprise any number of samples. Therefore, It would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teaching of Hedberg and admitted prior art for the purpose of having detection window with odd or even number of sample as suggested by Admitted Prior Art (Specification: page 3: line 2).

20. Claims 5, 7-8, 13, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hedberg in view of what is old and well known.

Regarding claim 5, Hedberg discloses as recited in rejection of claim 4 above. Hedberg is silent about filtering glitches or spikes in the bit stream. However, filtering out glitches or spikes in a bit stream is notoriously old in the subject matter area of the invention. (Kim et al. US 6,994,884: Abstract, col. 2: lines 52-60). It would have been obvious to include in Hedberg's bit stream decoding any old and well known filtering of glitches and spikes, since it is used in that environment and would make Hedberg's bit stream decoding more efficient.

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Regarding claim 13, Hedberg discloses as recited in rejection of claim 12 above.

Hedberg is silent about filtering glitches or spikes in the bit stream. However, filtering out glitches or spikes in a bit stream is notoriously old in the subject matter area of the invention. (Kim et al. US 6,994,884: Abstract, col. 2: lines 52-60). It would have been obvious to include in Hedberg's bit stream decoding any old and well known filtering of glitches and spikes, since it is used in that environment and would make Hedberg's bit stream decoding more efficient.

Regarding claim 17, Hedberg discloses as recited in rejection of claim 1 above. Hedberg is silent about use of data storage medium having instruction stored thereon. However, data storage medium having instruction stored thereon is notoriously old in the subject matter area of the invention. It would have been obvious to include in Hedberg's bit stream decoding any old and well known data storage medium having instruction stored thereon, since when it is used in that environment, it would provide Hedberg's bit stream decoding with more efficient means of implementation.

21. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. in view of what is old and well known.

Regarding claim 17, Clark et al. disclose as recited in rejection of claim 1 above. They are silent about use of data storage medium having instruction stored thereon. However, data storage medium having instruction stored thereon is notoriously old in

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the subject matter area of the invention. It would have been obvious to include in Clark et al. 's bit stream decoding any old and well known data storage medium having instruction stored thereon, since when it is used in that environment, it would provide Clark et al. 's bit stream decoding with more efficient means of implementation.

Allowable Subject Matter

22. Claims 3, 6, 11, 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Remarks

23. No claim is allowed.

Conclusion

- 24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jerrim et al. (US 4,653,076).
- 25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

- 26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
- 27. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.
- 28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nader Bolourchi whose telephone number is (571) 272-8064. The examiner can normally be reached on M-F 8:30 to 4:30.
- 29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David. C. Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

Nader Bolourchi
NS
2/1/2008

DAVID C. PAYNÉ SUPERVISORY PATENT EXAMINER